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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James Robert Kohn

Title: METHOD AND APPARATUS FOR INDIRECTLY ADDRESSED VECTOR LOAD-ADD-STORE ACROSS MULTI-PROCESSORS

Docket No.: 1376.731US1

Serial No.: 10/643,727

Filed: August 18, 2003

Due Date: N/A

Examiner: Unknown

Group Art Unit: 2121

MS Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- X Return postcard.
- X Communication Concerning Related Applications (1 pg.).
- X Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (5 pgs.), and copies of 41 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

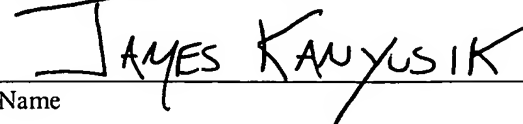
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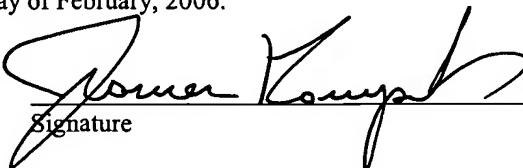
By: 

Atty: Thomas F. Brennan

Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of February, 2006.


Name


Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)



Serial 10/643,727

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James R. Kohn
Serial No.: 10/643,727
Filed: August 18, 2003
Title: METHOD AND APPARATUS FOR INDIRECTLY ADDRESSED VECTOR
LOAD-ADD-STORE ACROSS MULTI-PROCESSORS

Examiner: Unknown
Group Art Unit: 2121
Docket: 1376.731US1

COMMUNICATION CONCERNING RELATED APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/235,898	September 4, 2002	1376.710US1	REMOTE TRANSLATION
6,922,766			MECHANISM FOR A MULTI-NODE SYSTEM

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,
JAMES R. KOHN

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date Feb 17, 2006

By Thomas F. Brennan

Thomas F. Brennan
Reg. No. 35,075

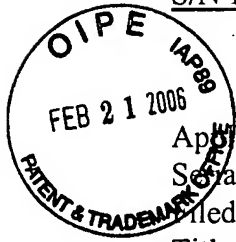
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of February, 2006.

JAMES KAUXSIK
Name

James Kauxsik
Signature

S/N 10/643,727

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	James Robert Kohn	Examiner:	Unknown
Serial No.:	10/643,727	Group Art Unit:	2121
Filed:	August 18, 2003	Docket:	1376.731US1
Title:	METHOD AND APPARATUS FOR INDIRECTLY ADDRESSED VECTOR LOAD-ADD-STORE ACROSS MULTI-PROCESSORS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/643,727

Filing Date: August 18, 2003

Title: METHOD AND APPARATUS FOR INDIRECTLY ADDRESSED VECTOR LOAD-ADD-STORE ACROSS MULTI-PROCESSORS

Page 2

Dkt: 1376.731US1

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any U.S. Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

JAMES ROBERT KOHN

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date Feb 17, 2006

By Thomas F. Brennan
Thomas F. Brennan
Reg. No. 35,075

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Name

JAMES KANYUSIK

Signature

James Kanyusik



Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

PTO/SB/08A(10-01)
 Approved for use through 10/31/2002. OMB 651-0031
 US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE

Complete if Known

Application Number	10/643,727
Filing Date	August 18, 2003
First Named Inventor	Kohn, James
Group Art Unit	2121
Examiner Name	Unknown

Sheet 1 of 5

Attorney Docket No: 1376.731US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-2002/0169938A1	11/14/2002	Scott, S. L., et al.	12/14/2001
	US-2002/0172199A1	11/21/2002	Scott, S. L., et al.	12/14/2001
	US-2003/0005380A1	01/02/2003	Nguyen, H. T., et al.	06/29/2001
	US-2005/0044128A1	02/24/2005	Scott, S. L., et al.	08/18/2003
	US-2005/0044340A1	02/24/2005	Sheets, K., et al.	08/18/2003
	US-4,541,046	09/10/1985	Nagashima, S., et al.	03/23/1982
	US-4,771,391	09/13/1988	Blasbalg, H.	07/21/1986
	US-4,868,818	09/19/1989	Madan, H. S., et al.	10/29/1987
	US-4,888,679	12/19/1989	Fossum, T., et al.	01/11/1988
	US-4,933,933	06/12/1990	Dally, W. J., et al.	12/19/1986
	US-5,008,882	04/16/1991	Peterson, J. C., et al.	08/17/1987
	US-5,031,211	07/09/1991	Nagai, Y., et al.	02/01/1990
	US-5,036,459	07/30/1991	Den Haan, P. A., et al.	03/09/1989
	US-5,068,851	11/26/1991	Bruckert, W., et al.	08/01/1989
	US-5,105,424	04/14/1992	Flaig, C. M., et al.	06/02/1988
	US-5,157,692	10/20/1992	Horie, T., et al.	03/20/1990
	US-5,161,156	11/03/1992	Baum, R. I., et al.	02/02/1990
	US-5,170,482	12/08/1992	Shu, R., et al.	02/13/1991
	US-5,175,733	12/29/1992	Nugent, S. F.	12/27/1990
	US-5,197,130	03/23/1993	Chen, S. S., et al.	12/29/1989
	US-5,218,601	06/08/1993	Chujo, T., et al.	12/20/1990
	US-5,218,676	06/08/1993	Ben-ayed, M., et al.	01/08/1990
	US-5,239,545	08/24/1993	Buchholz, D. R.	11/05/1990
	US-5,276,899	01/04/1994	Neches, P. M.	08/10/1990
	US-5,280,474	01/18/1994	Nickolls, J. R., et al.	01/05/1990
	US-5,313,628	05/17/1994	Mendelsohn, N. R., et al.	12/30/1991
	US-5,313,645	05/17/1994	Rolfe, D. B.	05/13/1991
	US-5,331,631	07/19/1994	Teraslinna, K. T.	03/16/1993
	US-5,333,279	07/26/1994	Dunning, D.	06/01/1992
	US-5,341,504	08/23/1994	Mori, K., et al.	03/01/1990
	US-5,347,450	09/13/1994	Nugent, S. F.	08/19/1993
	US-5,353,283	10/04/1994	Tsuchiya, P. F.	05/28/1993
	US-5,365,228	11/15/1994	Childs, P. L., et al.	08/21/1991
	US-5,418,916	05/23/1995	Hall, B. A., et al.	10/04/1990
	US-5,430,850	07/04/1995	Papadopoulos, G. M., et al.	07/22/1991
	US-5,430,884	07/04/1995	Beard, D. R., et al.	06/11/1990
	US-5,434,995	07/18/1995	Oberlin, S. M., et al.	12/10/1993
	US-5,440,547	08/08/1995	Easki, H., et al.	01/05/1994
	US-5,446,915	08/29/1995	Pierce, P. R.	05/25/1993
	US-5,517,497	05/14/1996	LeBoudec, J.-Y., et al.	03/21/1995

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. † Applicant's unique citation designation number (optional) ‡ Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number 10/643,727

Filing Date August 18, 2003

First Named Inventor Kohn, James

Group Art Unit 2121

Examiner Name Unknown

Sheet 2 of 5

Attorney Docket No: 1376.731US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-5,546,549	08/13/1996	Barrett, L., et al.	06/01/1994
	US-5,548,639	08/20/1996	Ogura, T., et al.	10/22/1992
	US-5,550,589	08/27/1996	Shiojiri, H., et al.	11/04/1994
	US-5,555,542	09/10/1996	Ogura, T., et al.	01/11/1996
	US-5,560,029	09/24/1996	Papadopoulos, G. M., et al.	05/31/1994
	US-5,640,524	06/17/1997	Beard, D. R., et al.	02/28/1995
	US-5,649,141	07/15/1997	Yamazaki, T.	06/30/1995
	US-5,787,494	07/28/1998	Delano, E. R., et al.	09/22/1995
	US-5,860,146	01/12/1999	Vishin, S., et al.	06/25/1996
	US-5,897,664	04/27/1999	Nesheim, W. A., et al.	07/01/1996
	US-6,003,123	12/14/1999	Carter, N. P., et al.	02/10/1998
	US-6,088,701	07/11/2000	Whaley, K. M., et al.	11/14/1997
	US-6,101,590	08/08/2000	Hansen, C.	10/10/1995
	US-6,105,113	08/15/2000	Schimmel, C. F.	08/21/1997
	US-6,490,671	12/03/2002	Frank, R. L., et al.	05/28/1999
	US-6,684,305	01/27/2004	Deneau, T. M.	04/24/2001
	US-6,782,468	08/24/2004	Nakazato, S.	12/13/1999
	US-6,816,960	11/09/2004	Koyanagi, H.	07/10/2001
	US-6,922,766	07/26/2005	Scott, S. L.	09/04/2002
	US-6,925,547	08/02/2005	Scott, S. L., et al.	12/14/2001
	US-6,976,155	12/13/2005	Drysdale, T. G., et al.	06/12/2001

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"Cray Assembly Language (CAL) for Cray X1™ Systems Reference Manual", Section 2.6, Memory Ordering, http://docs.cray.com/books/S-2314-51/index.html , (June, 2003), 302 pgs.	
		"Deadlock-Free Routing Schemes on Multistage Interconnection Networks", IBM Technical Disclosure Bulletin, 35, (December, 1992), 232-233	
		"ECPE 4504: Computer Organization Lecture 12: Computer Arithmetic", The Bradley Department of Electrical Engineering, (October 17, 2000), 12 pgs.	
		ABTS, D, "So Many States, So Little Time: Verifying Memory Coherence in the Cray X1", Parallel and Distributed Processing Symposium, (April 22, 2003), 11-20	
		ADVE, V. S., et al., "Performance Analysis of Mesh Interconnection Networks with Deterministic Routing", Transactions on Parallel and Distributed Systems, (March, 1994), 225-246	

EXAMINER

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2" style="padding: 2px;"><i>Complete if Known</i></td> </tr> <tr> <td style="width: 60%; padding: 2px;">Application Number</td> <td style="padding: 2px;">10/643,727</td> </tr> <tr> <td style="padding: 2px;">Filing Date</td> <td style="padding: 2px;">August 18, 2003</td> </tr> <tr> <td style="padding: 2px;">First Named Inventor</td> <td style="padding: 2px;">Kohn, James</td> </tr> <tr> <td style="padding: 2px;">Group Art Unit</td> <td style="padding: 2px;">2121</td> </tr> <tr> <td style="padding: 2px;">Examiner Name</td> <td style="padding: 2px;">Unknown</td> </tr> </table>	<i>Complete if Known</i>		Application Number	10/643,727	Filing Date	August 18, 2003	First Named Inventor	Kohn, James	Group Art Unit	2121	Examiner Name	Unknown
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		BOLDING, KEVIN, "Non-Uniformities Introduced by Virtual Channel Deadlock Prevention", <u>Technical Report 92-07-07, Department of Computer Science and Engineering, FR-35 University of Washington; Seattle, WA 98195</u> , (July 21, 1992), 6 pgs.	
		BOLLA, R., "A Neural Strategy for Optimal Multiplexing of Circuit and Packet-Switched Traffic", <u>Proceedings, IEEE Global Telecommunications Conference</u> , (1992), 1324-1330	
		BOURA, Y M., et al., "Efficient Fully Adaptive Wormhole Routing in <i>n</i> -dimensional Meshes", <u>Proceedings, International Conference on Distributed Computing Systems</u> , (June, 1994), 589-596	
		BUNDY, A., et al., "Turning Eureka Steps into Calculations in Automatic Program", <u>Proceedings of UK IT 90, (IEE Conf. Pub. 316) (DAI Research Paper 448)</u> , (1991), 221-226	
		CARLILE, BRADLEY R., "Algorithms and Design: The CRAY APP Shared-Memory System", <u>COMPCON Spring '93. Digest of Papers.</u> , (February 22, 1993), 312-320	
		CHEN, Y., et al., "UTLB: A Mechanism for Address Translation on Network Interfaces", <u>Proceedings of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)</u> , (1998), 193-204	
		CHIEN, A. A., et al., "Planar-Adaptive Routing: Low-Cost Adaptive Networks for Multiprocessors", <u>Proceedings, 19th International Symposium on Computer Architecture</u> , (May 1992), 268-277	
		DALLY, W. J., et al., "Deadlock-Free Adaptive Routing in Multicomputer Networks Using Virtual Channels", <u>IEEE Transactions on Parallel and Distributed Systems</u> , 4(4), (April, 1993), 466-475	
		DALLY, WILLIAM, et al., "Deadlock-Free Message Routing in Multiprocessor Interconnection Networks", <u>IEEE Transactions on Computers</u> , Vol. C-36, (May, 1987), 547-553	
		DALLY, WILLIAM, "Performance Analysis of <i>k</i> -ary <i>n</i> -cube Interconnection Networks", <u>IEEE Transactions on Computers</u> , 39(6), (June 1990), 775-785	
		DALLY, W. J., "Virtual Channel Flow Control", <u>Proceedings, 17th International Symposium on Computer Architecture</u> , (May, 1990) 60-68	
		DUATO, J., "A New Theory of Deadlock-Free Adaptive Routing in Wormhole Networks", <u>IEEE Transactions on Parallel and Distributed Systems</u> , 4(12), (December, 1993), 1320-1331	
		ERNST, D., et al., "Cyclone: A Broadcast-Free Dynamic Instruction Scheduler with Selective Replay", <u>30th Annual International Symposium on Computer Architecture (ISCA-2003)</u> , (June, 2003), 10 pgs.	
		GALLAGER, ROBERT, "Scale Factors for Distributed Routing Algorithm", <u>NTC '77 Conference Record, Vol. 2</u> , (1977), 28:2-1 - 28:2-5	

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
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		GLASS, C. J., et al., "The Turn Model for Adaptive Routing", <u>Proceedings, 19th International Symposium on Computer Architecture</u> , (May, 1992), 278-287	
		GRAVANO, L., et al., "Adaptive Deadlock- and Livelock-Free Routing with all Minimal Paths in Torus Networks", <u>IEEE Transactions on Parallel and Distributed Systems</u> , 5(12), (December, 1994), 1233-1251	
		GUPTA, RAJIV, et al., "High Speed Synchronization of Processors Using Fuzzy Barriers", <u>International Journal of Parallel Programming</u> 19(1), (February, 1990), 53-73	
		ISHIHATA, HIROAKI, et al., "Architecture of Highly Parallel AP1000 Computer", <u>Systems and Computers in Japan</u> , 24(7), (1993), 69-76	
		JESSHOPE, C. R., et al., "High Performance Communications in Processor Networks", <u>Proceedings, 16th International Symposium on Computer Architecture</u> , (May, 1989), 150-157	
		KIRKPATRICK, S., et al., "Optimization by Simulated Annealing", <u>Science</u> , 220(4598), (May 13, 1983), 671-680	
		KONTOTHANASSIS, L., et al., "VM-based Shared Memory on Low-Latency, Remote-Memory-Access Networks", <u>Proceedings of the ACM ISCA '97</u> , (1997), 157-169	
		LINDER, DANIEL H., et al., "An Adaptive and Fault Tolerant Wormhole Routing Strategy for <i>k</i> -ary <i>n</i> -cubes", <u>IEEE Transactions on Computers</u> , 40(1), (1991), 2-12	
		LUI, Z, et al., "Grouping Virtual Channels for Deadlock-Free Adaptive Wormhole Routing", <u>Fifth International Conference, Parallel Architectures and Languages Europe (PARLE '93)</u> , (June 14-17, 1993), 254-265	
		NUTH, PETER, et al., "The J-Machine Network", <u>Proceedings of the IEEE International Conference on Computer Design on VLSI in Computer & Processors</u> (1992), 420-423	
		O'KEEFE, MATTHEW T., et al., "Static Barrier MIMD: Architecture and Performance Analysis", <u>Journal of Parallel and Distributed Computing</u> , 25(2), (March 25, 1995), 126-132	
		PATTERSON, DAVID A., et al., <u>Computer Architecture: A Quantitative Approach</u> , Second Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, (1996), 39-41	
		PATTERSON, DAVID A., et al., <u>Computer Architecture: A Quantitative Approach</u> , Second Edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, (1996), 179-187, 373-384	
		SCOTT, S., "Synchronization and Communication in the T3E Multiprocessor", <u>ASPLOS, Volume II</u> , (1996), 26-36	
		SHUMWAY, M., "Deadlock-Free Packet Networks", <u>Transputer Research and Applications 2, NATUG-2 Proceedings of the Second Conference of the North American Transputer Users Group</u> , (October 18-19, 1989), 140-177	

EXAMINER

DATE CONSIDERED

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<div style="border: 1px solid black; padding: 2px; margin-bottom: 2px;">Complete if Known</div> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%; border: 1px solid black; padding: 2px;">Application Number</td> <td style="border: 1px solid black; padding: 2px;">10/643,727</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Filing Date</td> <td style="border: 1px solid black; padding: 2px;">August 18, 2003</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">First Named Inventor</td> <td style="border: 1px solid black; padding: 2px;">Kohn, James</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Group Art Unit</td> <td style="border: 1px solid black; padding: 2px;">2121</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Examiner Name</td> <td style="border: 1px solid black; padding: 2px;">Unknown</td> </tr> </table>	Application Number	10/643,727	Filing Date	August 18, 2003	First Named Inventor	Kohn, James	Group Art Unit	2121	Examiner Name	Unknown
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Group Art Unit	2121										
Examiner Name	Unknown										
Sheet 5 of 5	Attorney Docket No: 1376.731US1										

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SNYDER, L., "Introduction to the Configurable, Highly Parallel Computer", <u>IEEE Computer</u> , 15(1), (January, 1982), 47-56	
		TALIA, D., "Message-Routing Systems for Transputer-Based Multicomputers", <u>IEEE Micro</u> , 13(3), (June, 1993), 62-72	
		WANG, WEILIN, et al., "Trunk Congestion Control in Heterogeneous Circuit Switched Networks", <u>IEEE Transactions on Communications</u> , 40(7), (July, 1992), 1156-1161	
		WOOD, D. A., et al., "An In-Cache Address Translation Mechanism", <u>Proceedings of the 13th Annual International Symposium on Computer Architecture</u> , (1986), 358-365	
		WU, MIN-YOU, et al., "DO and FORALL: Temporal and Spatial Control Structures", <u>Proceedings, Third Workshop on Compilers for Parallel Computers, ACPC/TR</u> , July 1992, 258-269	
		YANG, C. S., et al., "Performance Evaluation of Multicast Wormhole Routing in 2D-Torus Multicomputers", <u>Proceedings, Fourth International Conference on Computing and Information (ICCI '92)</u> , (1992), 173-178	
		YANTCHEV, J., et al., "Adaptive, Low Latency, Deadlock-Free Packet Routing for Networks of Processors", <u>IEEE Proceedings</u> , 136, Part E, No. 3, (May, 1989), 178-186	

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DATE CONSIDERED